

## REMARKS

Claims 1-26 are pending in the application. Claims 1, 3-5, 7-8, 10-12, 14-16, 18-19 and 21-22 have been amended. In view of the following, all of the claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner schedule a teleconference with the Applicant's attorney to further the prosecution of the application.

### **Rejection of claims 1-26 under §112, second paragraph, as being indefinite**

The Examiner has indicated that claims 1-26 would be allowable if rewritten to overcome the rejection under §112, second paragraph.

#### **Claim 1**

Claim 1 has been amended to correct antecedent basis and clarify the connection of the first and second window circuits.

For example, referring, e.g., to FIG. 4 and paragraphs 22-28 of the present application, an oscillator 206 has an oscillator signal whose frequency is related to a received error correction signal. A phase-frequency detector 200 receives and compares the oscillator signal IN1 and a reference signal IN2 from a master circuit 112a, and generates the error correction signal received by the oscillator based on a phase difference of the oscillator signal IN1 and the reference signal IN2. A first window circuit (+N counter) 218 is coupled to the detector 200 and is operable to count a number of comparing cycles of the detector 200 and provide a first window signal WIN1 for a transmission of the error correction signals from the detector 200 to the oscillator 206 at a frequency of a predetermined number (+N) of counted comparing cycles. A second window circuit 300 (including 310 and 320) is coupled to the detector 200 and, in response to at least the oscillator signal IN1, is operable to narrow the first window signal WIN1 to limit a duration of the error correction signal for irregular reference signals IN2.

### **Claim 12**

Claim 12, as amended, is patentable for reasons similar to those recited above in support of the patentability of claim 1.

### **Claim 3**

Claim 3 has been amended to correct antecedent basis.

For example, referring, e.g., to FIG. 4 and paragraphs 22-28 of the present application, the second window circuit 300 (including 310 and 320) includes, for each of the oscillator signal IN1 and the reference signal IN2, a delayed path (through time delay 314 and inverter 316, or through time delay 324 and inverter 326) delayed with respect to a generally non-delayed path (around time delays 314 and 324) and a first logic circuit (NOR gates 312 and 322) responsive to signals on the delayed and the generally non-delayed paths to produce a second window signal WIN2 which narrows the first window signal WIN1.

### **Claims 7, 14 and 18**

Claims 7, 14 and 18, as amended, are patentable for reasons similar to those recited above in support of the patentability of claim 3.

### **Claim 4**

Claim 4 has been amended to correct antecedent basis.

For example, referring, e.g., to FIG. 4 and paragraphs 22-28 of the present application, the delayed paths (claim 3 recites that the second window circuit includes a delayed path for each of the oscillator signal and the reference signal) provide the oscillator signal IN1 and reference signal IN2 to the detector 200 for comparing.

### **Claim 15**

Claim 15, as amended, is patentable for reasons similar to those recited above in support of the patentability of claim 4.

**Claims 5, 8, 10, 16, 19 and 21**

Claims 5, 8, 10, 16, 19 and 21 have been amended to correct antecedent basis.

**Claims 6 and 17**

Claims 6 and 17 do not lack antecedent basis because claims 3 and 14 both recite that the second window circuit includes a delayed path for each of the oscillator signal and the reference signal.

**Claims 11**

Claim 11 has been amended to correct antecedent basis and clarify the connection of the rate selector.

For example, referring, *e.g.*, to FIGS. 8 and 9 and paragraphs 33-35 of the present application, a rate selector circuit 400 is coupled to the first window circuit 218 and operable to monitor and adjust the “predetermined number of counted comparing cycles” (from claim 1) as a function of the error correction signal.

**Claim 22**

Claim 22, as amended, is patentable for reasons similar to those recited above in support of the patentability of claim 11.

**Claims 2, 6, 9, 13, 17, 20 and 23-26**

Claims 2, 6, 9, 13, 17, 20 and 23-26 are patentable by virtue of their respective dependencies from independent claims 1 and 12.

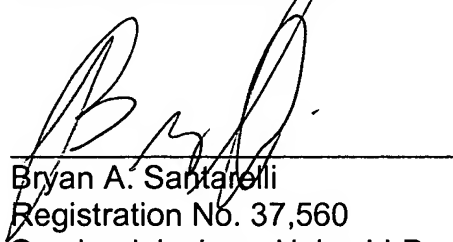
## CONCLUSION

In light of the foregoing remarks, claims 1-26 are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner contact the Applicants' attorney, Bryan Santarelli, at (425) 455-5575.

Respectfully submitted,



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